Claims

We claim:

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

4. The electronic structure of claim 1, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

5. The electronic structure of claim 1, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

6. The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

7. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

a solder member electrically coupling the first pad to the second pad; and

an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

8. An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;

an organic chip carrier having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

a solder member electrically coupling the first pad to the second pad; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

9. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2; and

a solder member electrically coupling the first pad to the second pad.

10. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3; and

a solder member electrically coupling the first pad to the second pad.

11. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0; and

a solder member electrically coupling the first pad to the second pad.

12. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

15. The electronic structure of claim 12, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

16. The electronic structure of claim 12, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

18. An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;

an organic chip carrier having a second electrically conductive pad thereon;

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

19. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon;

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

20. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.40 mm.

21. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

electrically coupling, by use of a solder member, the first pad to the second pad.

22. The method of claim 21, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

23. The method of claim 21, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

24. The method of claim 21, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

25. The method of claim 21, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

26. The method of claim 21, wherein the solder member includes a lead-tin alloy.

27. A method of forming an electronic structure, comprising:

forming a semiconductor chip having a first electrically conductive pad thereon;

forming an organic chip carrier having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

electrically coupling, by use of a solder member, the first pad to the second pad; and

placing an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

28. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad;

electrically coupling, by use of a solder member, the first pad to the second pad; and

placing an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

29. A method of forming an structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2; and

electrically coupling, by use of a solder member, the first pad to the second pad.

30. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3; and

electrically coupling, by use of a solder member, the first pad to the second pad.

31. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0; and

electrically coupling, by use of a solder member, the first pad to the second pad.

32. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon; and

electrically coupling, by use of a solder member, the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

33. The method of claim 32, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

34. The method of claim 32, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

35. The method of claim 32, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

36. The method of claim 32, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

37. The method of claim 32, wherein the solder member includes a lead-tin alloy.

38. A method of forming an electronic structure, comprising:

forming a semiconductor chip having a first electrically conductive pad thereon;

forming an organic chip carrier having a second electrically conductive pad thereon;

electrically coupling, by use of a solder member, the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

placing an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

39. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon;

electrically coupling, by use of a solder member, the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

placing an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

40. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon; and

electrically coupling, by use of a solder member, the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.40 mm.